CRESCENT HEART SOFTWARE

R4000A PROBING SUPPORT

FOR USE WITH 92DM75A PROBE ADAPTERS

FOR PROBING R4000MC, R4000PC, R4000SC,

R4400MC, R4400PC & R4400SC PROCESSORS

USING TEKTRONIX TLA7XX LOGIC ANALYZERS

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1. INTRODUCTION

This manual describes CHS951 R4000A disassembly support for probing MIPS PGA-package R4000MC, R4000PC, R4000SC, R4400MC, R4400PC and R4400SC processors using Tektronix TLA7xx logic analyzers having acquisition modules of at least 102 channels.

The support software is similar to that of the Tektronix 92DM75A product for the older DAS9200 and TLA5xx analyzers, except that it runs on the newer TLA7xx analyzers. The software is intended for current users of the 92DM75A product needing to continue to use the 92DM75A probe adapter and / or to probe the R4X00MC and R4X00SC processors using TLA7xx analyzers.

Note that other Crescent Heart Software products are available which provide more advanced support for probing R4X00PC processors when using DAS9200, TLA5xx or TLA7xx analyzers.

1.1 CONNECTION TO SYSTEM UNDER TEST

Connection to the R4X00 system under test is accomplished through the use of a Tektronix 92DM75A probe adapter. One version of the probe adapter is used for probing R4X00PC processors with PGA packages of 179 pins; another version is used for probing R4X00MC and R4X00SC processors which allow for connection of an external cache and have PGA packages of 447 pins.

> Note that the 92DM75A probe adapter makes no connection to external cache signals of the R4X00MC and R4X00SC processors. However, direct connection to the external cache signals can be made by the user; the CHS952 R4000B and CHS953 R4000C companion support products provide support for probing the external cache signals.

The 92DM75A probe adapter provides standard headers to which the probes of the logic analyzer attach in order to connect to the signals of the processor. Note that direct connection of the logic analyzer (i.e., without use of the probe adapter) to probe the main signals of the processor is not recommended; the probe adapter contains circuitry which monitors some of the processor's control signals and provides additional signals to the acquisition module to enable proper bus acquisition to take place.

The circuitry of the 92DM75A probe adapter obtains its power from the power provided to the processor being probed. The original circuitry of the 92DM75A requires 5 Volts; the original 92DM75A probe adapter is only suitable for probing 5 Volt processors. In order to probe 3.3 Volt processors, the 5 Volt circuitry must be replaced with 3.3 Volt circuitry. Contact Crescent Heart Software for information concerning 92DM75A probe adapter circuitry conversion.

1.2 INSTALLING DISASSEMBLER AND SUPPORT SOFTWARE

Install the new disassembly support software on the TLA7xx logic analyzer in the same manner that other software is installed on a Windows95 system: insert the disassembly support disk in the floppy disk drive (disk label facing to the front for a portable unit; disk label facing to the right for a rack-mount unit); click on the Windows95 **Start** button; choose **Settings...**; choose **Control Panel**; double-click on **Add/Remove Programs**; click on **Install...** under the **Install/Uninstall** tab; then follow the on-screen directions.

Prior to installing the disassembly support software, remove any extant version of that same software (e.g., any earlier version). When in **Add/Remove Programs**, review the list of programs already present in the system. If a version of the support software already exists, select it and click on **Remove**. Once removal is complete, continue on to install the new software then as instructed in the preceding paragraph.

Note that no saved setup files (demonstration refmems) have been provided showing example acquisitions.

1.3 ABOUT THIS MANUAL

This manual is organized as follows:

Section 1: Introduction - Presents general information on installing disassembler software and manual organization.

Section 2: Setting Up The Hardware - Discusses probe adapter issues, including configuring the probe adapter jumpers.

Section 3: Configuring The Acquisition Module - Information is provided on setting up the acquisition module in preparation for data acquisition and disassembly display.

Section 4: Disassembly Display Of Data - Discusses how to view data, principally using the disassembly display.

Section 5: Acquisition Clocking Choices - A discussion of the acquisition clocking choices available and their uses.

Appendix A: Channel Assignments

Appendix B: Warranty And Service

2. SETTING UP THE HARDWARE

Connection to the R4X00 system under test is accomplished through the use of a Tektronix 92DM75A probe adapter. Refer to the Tektronix 92DM75A Instruction Manual in conjunction with the information presented herein.

2.1 ACQUISITION MODULE PROBES

2.1.1 TLA7xx Probing

The 102-channel TLA7xx acquisition module has two (2) probes not present on the 92A96 and 92C96 acquisition modules used with the DAS9200/TLA5xx. These are the **Q** probes (**Q0** and **Q1**); they are in addition to the **A0**, **A1**, **A2**, **A3**, **C0**, **C1**, **C2**, **C3**, **D0**, **D1**, **D2**, **D3**, **CK0**, **CK1**, **CK2** and **CK3** probes also present. The **Q** and **CK** probes are individual (single-channel) probes, while all other probes are eight-channel probes.

The 136-channel TLA7xx acquisition module (which can instead be used) adds **E0**, **E1**, **E2**, **E3**, **Q2** and **Q3** probes. The **E** probes are eight-channel probes.

> Note that on the TLA7xx all probes are capable of synchronous and asynchronous acquisition, including the **CK0**, **CK1**, **CK2** and **CK3** probes.

2.1.2 Probe Connections

The 92DM75A probe adapter provides no headers to connect the **Q** (or **E**) probes; these probes are left disconnected (unless used to probe miscellaneous signals of the system under test (SUT)).

All other probes should be connected as indicated on the probe adapter PCB, with the exception of swapping the **A0** and **D2** probes (i.e., plug the **A0** probe where the PCB indicates the **D2** probe should go, and plug the **D2** probe where the PCB indicates the **A0** probe should go), and also swapping the **A1** and **D3** probes.

2.2 PROBE ADAPTER JUMPERS

2.2.1 TClock0/TClock1 Jumpers

The **TClock0** jumper (J1412) and the **TClock1** jumper (J1421) continue to be used to delay when necessary the rising edge of **TClock** to properly clock the acquisition module as well as the probe adapter circuitry. Note that each of the two processor clock signals are used: **TClock0** is used to clock the acquisition module, and **TClock1** is used to clock the probe adapter circuity.

The jumpers should be set as they were set when using the DAS9200 or TLA5xx analyzer, as described in the 92DM75A Instruction Manual. The following is a review of the procedure.

The jumpers are to be placed in the "N" position if the rising edge of **TClock** occurs around the end of the bus cycle (that is, around the time of occurrence of the rising edge of **MasterClock**). This occurs when the SUT connects **SyncOut** directly to **SyncIn**.

When the SUT has a buffer present between **SyncOut** and **SyncIn**, the time of occurrence of **TClock** (as well as **RClock** and other clock signals) gets shifted to occur earlier in the bus cycle (by the amount of the delay of the buffer). In this case the probe adapter **TClock0** and **TClock1** jumpers must be set so that the rising edge of the **TClock** signals provided to the acquisition module and to the probe adapter circuitry are appropriately delayed, with the result that the clocking occurs around the time of the end of the bus cycle. Note that the delay settings of the **TClock0** and **TClock1** jumpers should be set to be the same.

2.2.1.1 Clockedge Timing Determination And Adjustment -

In order to properly set the positions of the probe adapter jumpers, the relative timing of the delayed **TClock** and **MasterClock** signals can be determined as follows. Connect an unused probe (such as **Q0**) to the **MasterClock** signal (found on the **Aux** header of the probe adapter) and its neighboring ground signal. Load the R4000A ***timing.tla*** saved setup file, and perform an asynchronous acquisition of the processor signals' activity (refer to Section 5.3, *Internal Clocking*).

Using the TLA7xx MagniVu capability to display asynchronous activity with 0.5 ns resolution in the vicinity of the acquisition trigger, determine the timing relationship between the rising edge of the **CK3** probe (delayed **TClock0**) and **MasterClock**. The time difference between the rising clock edges is determined by the delay of the **SyncOut-SyncIn** buffer as well as by the delay provided by the setting of the probe adapter **TClock0** jumper.

Change the probe adapter **TClock0** jumper position so that additional delay is provided; then reacquire the processor signal activity and determine what the current **CK3-MasterClock** edge timing difference is. Continue in an iterative manner until the timing difference has been minimized. Finally, be sure to set the position of the **TClock1** jumper to match that of the **TClock0** jumper.

Note that the processor does not have a well-defined output signal hold time relative to the rising edge of **MasterClock** (and/or **TClock**). (It may even be possible for processor output signals to start changing to their new state prior to the occurrence of the rising edge of **MasterClock**). Thus, adjusting the probe adapter delays so that sampling (by the probe adapter circuitry and by the acquisition module) occurs around the rising edge of **MasterClock** is not a guarantee that proper processor signal sampling will in fact occur.

Therefore, when synchronous acquisition is first attempted, it is recommended that the acquired signals' values be examined to determine whether reliable sampling is occurring. If not, the probe adapter **TClock0** and **TClock1** jumpers should be changed and a new acquisition obtained; some iteration may be required here.

In this process it will be helpful to monitor the **CK3-MasterClock** timing difference when the positions of the jumpers are changed (as descibed above, using asynchronous acqusition), in order to track what the clock edge timing relationships.

It will be helpful when performing the initial **CK3-MasterClock** asynchronous acquisitions to also examine the (asynchronous) timing of the various processor output signals, so that it may be determined where at the end of the bus cycle reliable probing can be expected to be achieved. Likewise, examine the timing of the signals supplied to the processor from the external SUT circuitry.

2.2.2 Normal/Timing Jumper -

The Normal/Timing jumper (J1411) continues to be used to control the behavior of the circuitry on the probe adapter.

The jumper is used in order to synchronously clock certain processor control signals and provide them and related derived signals to the acquisition module for use in synchronous acquisition (Normal mode), or to asynchronously pass processor control signals through to the acquisition module for asynchronous acquisition (Timing mode).

3. CONFIGURING THE ACQUISITION MODULE

This section provides information on setting up the acquisition module in preparation for data acquisition and disassembly display.

Information is provided on the following:

- loading support software
- channel groupings
- clocking choices
- symbols and symbol tables
- triggering

3.1 LOADING SUPPORT SOFTWARE

Assuming the software has already been installed on the analyzer (i.e., copied from floppy disk to the hard drive of the system; refer to Section 1.2, *Installing Disassembler And Support Software*), the software can then be loaded into the acquisition module.

In order to get ready to perform a disassembly acquisition the support software must be loaded into the acquisition module: select **Load Support Package...** from the **File** menu and select **R4000A** (found in the **C:\Program Files\TLA700\Supports** folder).

With the load performed, the LA module Setup window will show relevant acquisition-related information concerning: what channel groupings have been setup; the clocking mode; the memory depth; etc. Changes to these parameters can be made also via the LA module Setup window.

Figure 3.1 shows the LA module Setup window.

3.2 CHANNEL GROUPINGS

The disassembler software automatically defines the channel groups for the signals of the processor. The channel groups defined include: **SysAD**, **Data(Hi)**, **A**, **Addr(Lo)**, **Control**, **Intr**, **Ack**, **Misc**, **Chk**, **Clk** and **Unused**. Refer to the LA module Setup window to view or change the channel assignments; also refer to the channel assignment tables in Appendix A, *Channel Assignments.*

Proper operation of the disassembler generally requires that the definition of the **Data(Hi)**, **A**, **Addr(Lo)** and **Control** groups not be changed and the channels of these groups not be transferred to other groups or swapped with channels of other groups. (For more detailed information refer to Appendix A, *Channel Assignments.*)

Additional groups can be defined and displayed and nonessential groups can be changed or removed as desired. Note that with the exception of the specific channels in the required groups, a channel need not belong to a group.

Changes to the default values of threshold voltage (1.5 V: viewable under **Set Thresholds...** on the LA module Setup window) of any of the channels of the four required groups will likely adversely affect disassembly acquisition.

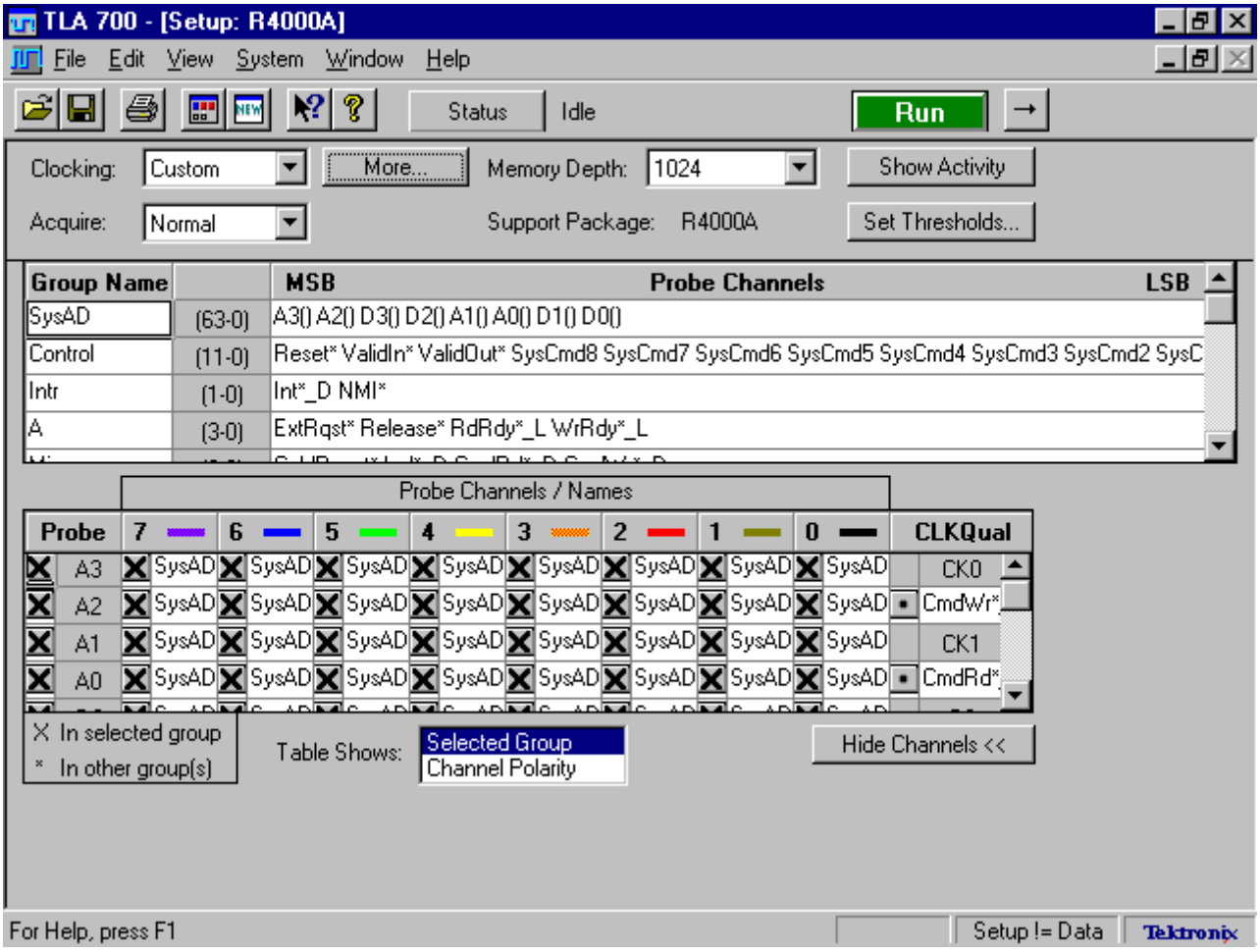

Figure 3.1 - LA Module Setup Window

3.3 CLOCKING CHOICES

The **Clocking** selection on the LA module Setup window can be used to set clocking choices to control data acquisition. The disassembler software provides a **Custom** clocking selection which is the default setup.

In addition to **Custom** clocking, **Internal**, **External** and **Advanced** clocking can be selected. These clocking choices are not used for disassembly acquisition; refer to Section 5, *Acquisition Clocking Choices*, for an explanation of their use.

The **Acquire** selection on the LA module Setup window allows the choice of **Normal**, **Blocks** and **Glitches** (for **Internal** clocking only) modes of acquisition. For disassembly acquisition, **Acquire** should be set to **Normal**. (**Blocks** mode, used in conjunction with a user-specified trigger program, may also be useful in certain situations.)

One **Custom** clock option field exists under the (clocking) **Options** selection of the LA module Setup window as described below. Refer to Figure 3.2.

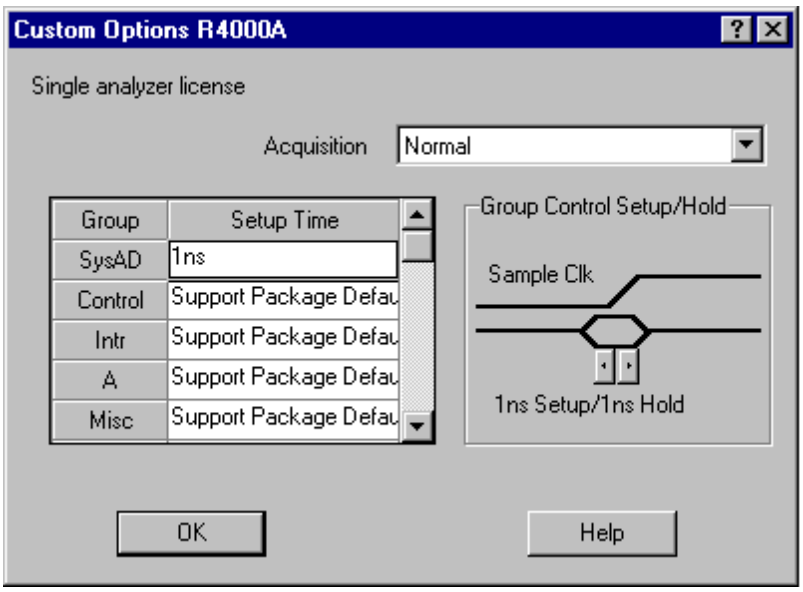

Figure 3.2 - LA Module Setup Window Custom Clocking Options

3.3.1 Acquisition Field

The selection chosen here determines how the clocking state machine (CSM) of the acquisition module will acquire bus cycles. Acquired bus cycles are passed to the trigger program (refer to Section 3.5, *Triggering*) for possible storage in acquisition memory.

Under **Normal** (the default selection), the acquisition module utilizes certain signals as qualifiers to control the acquisition process. This allows efficient acquisition of only those bus cycles which are useful in tracking the behavior of the processor. The **ValidIn***, **ValidOut***, **RdRdy*_L**, **WrRdy*_L**, **CmdRd*_D**, **CmdWr*_D** and **Ivd*_D** signals are used as qualifiers.

> Circuitry on the probe adapter produces the five last-named signals using signals produced by the processor or SUT: **RdRdy*_L** is produced from **RdRdy***; **WrRdy*_L** is produced from **WrRdy***; **CmdRd*_D** and **CmdWr*_D** are produced from the **SysCmd** signals; **Ivd*_D** is produced from **IvdAck*** and **IvdErr*** (all three of which are unasserted (electrically high) when probing R4X00PC processors). Likewise, the **Int*_D** signal is produced by the probe adapter from the **Int5***, **Int4***, **Int3***, **Int2***, **Int1*** and **Int0*** signals (note that **Int*_D** is not used as a qualifier).

Under **Acquire All Cycles**, the acquisition module acquires all bus cycles (note again that acquired bus cycles are passed to the trigger program for possible storage in acquisition memory). In this case the seven qualifier signals are ignored and have no influence concerning the acquisition process by the CSM.

The all-cycles acquisition capability is intended mainly for use in conjunction with state and timing displays (refer to Section 4.4.1, *State Display*, and Section 4.4.2, *Timing Display*); for disassembly displays the usual choice is **Normal** acquisition.

3.3.2 Clocking Delay

Please refer to the note at the end of this section, explaining that this information is presented for reference purposes only; it is recommended that the clocking delay (setup time) adjustment provided by the logic analyzer should remain set at the default value.

In order to insure reliable acquisition of bus signals in the face of signal skew, the timing (placement) of the clock edge can be effectively advanced or delayed internally by the analyzer before being used to sample the signals.

Figure 3.2 shows that the **Custom Clocking Options** window provides means to set the setup time associated with each defined channel group of the disassembler support. Note that while a unique setup time relative to the clock source's clock edge can be defined for each separate group, a shift in the apparent overall time of occurrence of the clock edge requires that the setup times for all groups be set uniformly to the same value.

The setup time shown under the Setup Time column is initially the "Support Package Default", which is a setup time of 2 ns. For such a setup time, the signals being acquired by the logic analyzer must be stable 2 ns before the clock source's edge (2 ns setup time) and must remain stable until the clock edge has occurred (0 ns hold time); the signals must exhibit a 2 ns window-of-stability which ends with the occurrence of the clock edge. This default value is a clocking delay (change in the acquisition sample point from the edge of the clock source) of 0 ns.

If a non-zero clocking delay is required, the setup times of all groups are changed appropriately. For example, if a clocking delay of 1 ns is required, the acquisition window-of-stability must be delayed in time by 1 ns. This is accomplished by changing the setup time from 2 ns to 1 ns (with a corresponding change in the hold time from 0 ns to 1 ns).

The setup time for a particular group can be accessed by clicking in the box corresponding to that group under the Setup Time column. Then, the two buttons under the timing waveforms graphic can be used to select the setup/hold time combination required. Setup time values ranging from 8.5 ns (an advance of 6.5 ns compared to the default setup time of 2 ns) to -7 ns (a delay of 9 ns compared to the default) in increments of 0.5 ns can be specified. Figure 3.2 shows the case where the setup time for the **SysAD** group has been changed to 1 ns.

Note that the extent of the window-of-stability remains 2 ns no matter what the setup time chosen is. Note also again that it should be verified that all groups are set to have the same setup time value.

> The above information is presented for reference purposes only. It is recommended that the clocking delay (setup time) adjustment provided by the logic analyzer should remain set at the default value.
>
> This is because there are two signal samplings which must take place: one by the logic analyzer acquisition module, and one by circuitry on the probe adapter. The clocking delay adjustment described above affects only the sampling of the acquisition module and has no effect upon the clocking of the probe adapter circuitry.
>
> Therefore it is recommended that the default setup times be used (2 ns setup, 0 ns hold) for the clocking delay, and that any clock edge time shifting be accomplished through the use of the **TClock0** and **TClock1** jumpers as described in Section 2.2.1, *TClock0/TClock1 Jumpers* (as would have been done when using the probe adapter with a DAS9200 or TLA5xx logic analyzer).
>
> Again, it is recommended that the clocking delay (setup time) adjustment provided by the logic analyzer should remain set at the default value.

3.4 SYMBOLS AND SYMBOL TABLES

This software support product provides symbol tables for use in display of the **Control**, **Intr** and **Ack** groups. The symbol tables are the same as found in the 92DM75A support software; refer to the 92DM75A Instruction Manual for related information.

3.5 TRIGGERING

Refer to the Setup subsection of the Reference section of the Analyzer Manual for general information concerning triggering and trigger programs.

Trigger programs can check the values of the various defined groups as well as the values of individual probe channels. Note that the groups' values used are those which have been acquired from the processor (not to be confused with disassembler-synthesized values displayed for some of the groups, as explained in Section 4.2, *Understanding The Disassembly Display*).

Beyond basic logical equality or non-equality checks, the trigger program can employ "range matching" to determine whether the value of a group is arithmetically greater than (or equal to), or less than (or equal to) a specified value. Range matching would usually be of interest for the **SysAD** lines which specify the address of the memory access. The **Addr(Lo)** group is composed of the lower 32 **SysAD** lines; the **Data(Hi)** group is composed of the upper 32 **SysAD** lines. Use of either of these groups allows range matching to be performed on the lower (or upper) **SysAD** lines.

The **SysAD** group, representing all 64 **SysAD** lines, has been defined to allow range matching to be carried out on the complete (64-bit) **SysAD** value. (This group is not used by the disassembler and is not required to be defined; it is redundant in the sense that between the **Data(Hi)** and **Addr(Lo)** groups (which are used by the disassembler) all **SysAD** lines already have group representation.)

> Note that the ordering of the analyzer channels for the purposes of arithmetic range matching is as follows: **C3**, **C2**, **C1**, **C0**, **E3**, **E2**, **E1**, **E0**, **A3**, **A2**, **D3**, **D2**, **A1**, **A0**, **D1**, **D0**, **Q3**, **Q2**, **Q1**, **Q0**, **CK3**, **CK2**, **CK1** and **CK0** (where, for example, **C3** represents the eight channels of the **C3** probe, #7..0; **Q3** represents the Qualifier #3 channel, and **CK3** represents the Clock #3 channel (note that all channels, including Clocks, acquire data)). For modules of widths other than 136-channels the channels which are not implemented are ignored (for example, for a 102-channel module **E3**, **E2**, **E1**, **E0**, **Q3** and **Q2** are not present).

When performing a disassembly (or other) acquisition, be sure to set the **Trigger Pos** setting on the LA module Trigger window as desired.

The most common use of triggering in conjunction with disassembly acquisition and display is to control when the start of data acquisition occurs (e.g., following the end of **ResetB** assertion, or after a processor request to read or write a particular memory location). Use of the triggering mechanism to "filter out" certain bus cycles from acquisition memory (e.g., to retain only write request bus cycles) results in "gaps" in the acquisition; the disassembly display will likely be adversely affected.

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4. DISASSEMBLY DISPLAY OF DATA

Information is provided here on how to acquire data and view it, principally using the disassembly display. The following are discussed:

- acquiring data
- understanding the disassembly display
- disassembly format definition overlay
- alternative data displays

4.1 ACQUIRING DATA

After loading the disassembler support software, choosing **Custom** clocking and possibly setting various clocking options in the LA module Setup window, and possibly configuring a trigger program in the LA module Trigger window, data can be acquired. Click on the **Run** button in the main window toolbar to start acquisition. Click on the same button when labeled **Stop** to stop acquisition if necessary.

4.2 UNDERSTANDING THE DISASSEMBLY DISPLAY

The disassembler provided with this probing support package has essentially the same functionality as the 92DM75A disassembler; refer to the 92DM75A Instruction Manual for information related to the functioning of the disassembler.

When a listing window is opening with a disassembly display, the address of the memory location being fetched appears under the **R4000A Addr(Lo)** column. The contents of the memory location and the disassembled instruction mnemonic display of the memory location contents appear under the **R4000A Data-Mnemonics** column.

> Note that with the 92DM75A support running on DAS9200 and TLA5xx analyzers, **Addr(Lo)**, **Data-Mnemonics** and all other columns appear with no preceding "**R4000A**" in the title.

It is important to understand that the disassembler controls not only what is displayed under the **R4000A Data-Mnemonics** column but also what is displayed under the **R4000A Addr(Lo)** column. In fact, any column named "**R4000A...**" (such as **R4000A Data(Hi)**, **R4000A A**, **R4000A Addr(Lo)**, **R4000A Data-Mnemonics**, etc.) presents information synthesized by the disassembly software; this is as opposed to columns having names without "**R4000A...**" (such as **Data(Hi)**, **Addr(Lo)**, **Intr**, etc.) which can also be displayed and which present the raw data as it was acquired.

Display of both types of information (synthesized and raw) can be enabled in one display at the same time as desired. Note that there is no "raw" version of the information presented under the **R4000A Data-Mnemonics** column. Also note that for example no "**R4000A...**" version of **Intr** can be displayed because the disassembler does not synthesize a version of that and some of the other groups. A listing display consisting of just the raw groups' data is termed a State display; no disassembly interpretation or synthetic group values are involved.

4.3 DISASSEMBLY FORMAT DEFINITION OVERLAY

The Disassembly properties page, referred to also as the disassembly format definition overlay, provides a number of fields whose settings control the operation of the disassembler and the display of disassembled data. The fields of the overlay have the same function as with the 92DM75A software product; see Figure 4.1 and refer to the 92DM75A Instruction Manual.

4.4 ALTERNATIVE DATA DISPLAYS

Bus cycle information that has been acquired using the **Custom** clocking selection (refer to Section 3.3, *Clocking Choices*) can be viewed not only using a disassembly display but also a state or even a timing display.

4.4.1 State Display

A state display is simply a variety of disassembly display in which only raw (non-synthesized) group values are selected for display

> Recall, as explained in Section 4.2, *Understanding The Disassembly Display*, that the values displayed under the **R4000A Data(Hi)**, **R4000A A**, **R4000A Addr(Lo)** and **R4000A Data-Mnemonics** groups' columns are software-synthesized for the disassembly display. Refer also to Appendix A, *Channel Assignments.*

A state display is most helpful in presenting the actual cycle-by-cycle values which occurred on the bus, since no data translation is performed.

4.4.2 Timing Display

The timing display, like the state display, presents the actual cycle-by-cycle values which occurred on the bus; no disassembly-like data translation is performed.

Use of the timing display may be helpful when the cycle-by-cycle behavior of particular individual channels (for example, **ResetB**) needs to be observed.

Generally, with information acquired using the **Custom** clocking selection, the timing display is only truly useful when the **Acquire All Cycles** selection of the **Acquisition** field of the **Custom Clocking Options** window has been chosen (refer to Section 3.3.1, *Acquisition Field*). Since such an acquisition is a record of all bus cycles (not just the principal cycles in which memory transaction request and data information are communicated, as would be acquired with a **Normal** selection in the **Acquisition** field), the timing display can be used to see a graphical cycle-by-cycle presentation of the behavior of the bus.

It is important to note that such a display is the result of synchronously sampling the bus signals; the display never shows signals changing except around the start of each bus cycle. In order to obtain a display which reveals the actual (intra-cycle) timing behavior of the signals, an asynchronous acquisition must be performed; refer to Section 5.3, *Internal Clocking*.

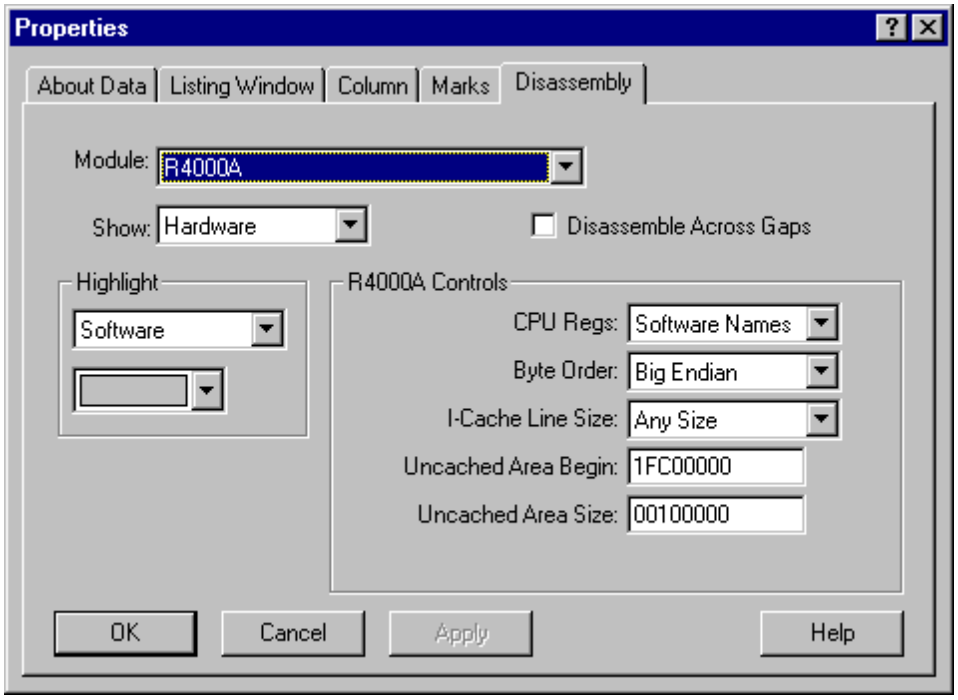

Figure 4.1 - Disassembly Properties Page

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5. ACQUISITION CLOCKING CHOICES

Besides the **Custom** clocking selection in the LA module Setup window which is utilized when acquiring data for disassembly display, other clocking selections are possible. Presented here is a discussion of the choices available and their uses.

5.1 CUSTOM CLOCKING

Acquisition of processor bus cycle information is usually done using the **Custom** clocking selection of the LA module Setup window. This is a form of synchronous acquisition in which a clock signal (**TClock**) obtained from the system under test (SUT) is used to clock the acquisition module.

Custom clocking is an LA module Setup window choice when the R4000A support has been loaded. **Custom** clocking implements a *clocking state machine* (CSM) which tracks the behavior of important bus control signals (termed *clock qualifiers*) and controls which bus samples are acted upon by the acquisition module's trigger program and are possibly stored in acquisition memory. **Custom** clocking also provides a set of clocking options (accessed via "More") in the LA module Setup window (refer to Figure 3.2, *LA Module Setup Window Custom Clocking Options*); these are inputs to the CSM which control its mode of operation.

> **Custom** clocking also implements a set of *pipeline delays* internal to the acquisition module; the setting of the pipeline delays allows the delays introduced by the probe adapter circuitry when synchronously producing certain signals (**ValidIn***, **ValidOut***, **RdRdy*_L**, **WrRdy*_L**, **CmdRd*_D**, **CmdWr*_D**, **Ivd*_D** and **Int*_D**) to be compensated for.
>
> The result is that all signals acquired by the acquisition module are given the same relative delay when they are passed to the trigger program for possible storage in acquisition memory. Therefore, a synchronous acquisition, and in particular an all-cycles acquisition, can be meaningfully displayed as a timing display, with all the signals' (synchronous) timing relationships properly indicated.
>
> Note that this result is quite different from the behavior of the 92DM75A support product running on the DAS9200 and TLA5xx, where the acquisition timing of certain signals (**Reset***, **Coldreset***, **SysADC7** and **SysADC3**) was adversely affected. Due to the manner in which the pipeline delays were configured on those analyzers, the named signals were acquired one cycle prior to all other signals. (Since the signals were not of great significance for disassembly acquisition and display, this uaually did not cause much of a problem.)

Besides **Normal Custom** clocking acquisition, a **Blocks Mode** of acquisition is also available which might be used to advantage in some situations in conjunction with a user-specified trigger program. In **Blocks Mode** each sample which is chosen for storage by the trigger program has a set of 31 additional samples stored preceding and following the sample (a total block of 63 samples is stored).

> Note that all such block-stored samples are samples which the CSM has qualified (or will qualify) to be passed on to the trigger program based on the settings of the **Custom** clocking options. The block-store samples are not taken from the raw (each cycle) behavior as seen on the bus and as input to the logic analyzer front end.
>
> Use of **Blocks Mode** should be considered carefully; unless utilized properly, it may tend to confuse the bus activity analysis when employed in conjunction with disassembly acquisition and display.

5.2 EXTERNAL CLOCKING

The LA module setup window provides an **External** clocking selection. This may be thought of as a simplified version of **Custom** clocking. Like **Custom** clocking, **External** clocking involves synchronous acquisition. However, rather than a software-configured CSM, a graphical user interface is provided which allows entry of a set of *clocking equations* involving the clock channels and clock qualifiers (no state machine capability is available).

Under **External** clocking a further choice of **Advanced** is possible in which the settings of additional hardware capabilities (multiple clocks, multiplexing, pipeline delay and setup times) can be specified. **External** clocking also provides a **Blocks Mode** of acquisition.

> Note that no CSM qualification of the block-store samples occurs, since under **External** clocking no CSM exists.

Generally, with the support software loaded there is little utility in employing **External** clocking.

5.3 INTERNAL CLOCKING

The LA module Setup window provides an **Internal** clocking selection. **Internal** clocking involves asynchronous acquisition; a free-running clock in the acquisition module times data acquisition. The LA module Setup window provides a field with which the internal clock rate can be set. Under **Internal** clocking, no set of clocking equations or CSM exists to control the acquisition process.

The timing display is most usually used to view processor bus activity which has been acquired using **Internal** clocking.

Probably the easiest way to get ready to perform an **Internal** clocking acquisition to be viewed as a timing display is to load an already-available system setup file: select **Load System** from the **File** menu, and then select the setup file (**.tla** file extension) desired. For example, the ***timing.tla*** file supplied with the disassembly support can be loaded (found in the **C:\Program Files\TLA700\Supports\R4000A** folder). The display will show signals listed in an appropriate ordering (which can be changed as desired). An acquisition then performed will display in the same data waveform window, retaining the already-defined signal ordering.

Internal clocking, like **Custom** and **External** clocking, also provides a **Blocks Mode** of acquisition. As described in Section 5.1, *Custom Clocking*, 62 additional samples are stored when the trigger program decides to store a sample in acquisition memory.

> Note that no CSM qualification of the block-store samples occurs, since under **Internal** clocking no CSM exists.

A. CHANNEL ASSIGNMENTS

The channel assignment information presented here in table form reflects the default state of the LA module Setup window once the support software is loaded. The channels of each group are listed in order from most-significant bit (MSB) to least-significant bit (LSB).

All channels are defined by the support software to have 1.5 V thresholds. Channels marked in the tables with a suffix of "*****" (not to be confused with signal names containing "*") are utilized as clock qualifiers by the acquisition module clocking state machine (CSM) and are required for proper **Custom** clocking acquisition.

A.1 DATA(HI) GROUP

The default radix of the group is **HEX**. The default radix for disassembly display is **OFF**.

The disassembler synthesizes the values displayed under the **R4000A Data(Hi)** group column (independent of the channels' actual values); displayed are the values of the **SysAD63..32** signals as emitted during the memory transaction's access request bus cycle.

Refer to Table A.1.

Bit Position	Channel	Signal Name
31	A3:7	SysAD63
30	A3:6	SysAD62
29	A3:5	SysAD61
28	A3:4	SysAD60
27	A3:3	SysAD59
26	A3:2	SysAD58
25	A3:1	SysAD57
24	A3:0	SysAD56
23	A2:7	SysAD55
22	A2:6	SysAD54
21	A2:5	SysAD53
20	A2:4	SysAD52
19	A2:3	SysAD51
18	A2:2	SysAD50
17	A2:1	SysAD49
16	A2:0	SysAD48
15	D3:7	SysAD47
14	D3:6	SysAD46
13	D3:5	SysAD45
12	D3:4	SysAD44
11	D3:3	SysAD43
10	D3:2	SysAD42
9	D3:1	SysAD41
8	D3:0	SysAD40
7	D2:7	SysAD39
6	D2:6	SysAD38
5	D2:5	SysAD37
4	D2:4	SysAD36
3	D2:3	SysAD35
2	D2:2	SysAD34
1	D2:1	SysAD33
0	D2:0	SysAD32

Table A.1 - Data(Hi) Group Channel Assignments

A.2 A GROUP

The default radix of the group is **OFF**. The default radix for disassembly display is **OFF**.

The disassembler requires that a group with the name "**A**" exists, and the group is required to have four channels in it. Any channel(s) can be used to make up the group. Usually the group will be composed of the processor control signals shown below.

During disassembly display the disassembler synthesizes the values displayed under the **R4000A A** group column (independent of the channels' actual values); displayed are the upper physical address bits issued during the memory access request cycle (which are interpreted in conjunction with the low 32 address bits displayed under the **Addr(Lo)** group column).

Refer to Table A.2.

Bit Position	Channel	Signal Name
3	C1:5	ExtRqst*
2	C1:1	Release*
1	C2:1*	RdRdy*_L
0	C2:0*	WrRdy*_L

Table A.2 - A Group Channel Assignments

A.3 ADDR(LO) GROUP

The default radix of the group is **HEX**. The default radix for disassembly display is **HEX**.

The group and all channels as listed are required for use by the disassembler to produce a disassembly display.

During disassembly display the disassembler synthesizes the values displayed under the **R4000A Addr(Lo)** group column, independent of the channels' actual values.

Refer to Table A.3.

A.4 SYSAD GROUP

The default radix of the group is **OFF**. The default radix for disassembly display is **OFF**.

This 64-channel group is composed of the 32 channels of the **Data(Hi)** group together with the 32 channels of the **Addr(Lo)** group. The group's value is not synthesized by the disassembler; its value is that of the acquired signals.

The group is defined to facilitate trigger program range matching on any or all of the **SysAD** signals.

The group is not required for use by the disassembler.

Bit Position	Channel	Signal Name
31	A1:7	SysAD31
30	A1:6	SysAD30
29	A1:5	SysAD29
28	A1:4	SysAD28
27	A1:3	SysAD27
26	A1:2	SysAD26
25	A1:1	SysAD25
24	A1:0	SysAD24
23	A0:7	SysAD23
22	A0:6	SysAD22
21	A0:5	SysAD21
20	A0:4	SysAD20
19	A0:3	SysAD19
18	A0:2	SysAD18
17	A0:1	SysAD17
16	A0:0	SysAD16
15	D1:7	SysAD15
14	D1:6	SysAD14
13	D1:5	SysAD13
12	D1:4	SysAD12
11	D1:3	SysAD11
10	D1:2	SysAD10
9	D1:1	SysAD9
8	D1:0	SysAD8
7	D0:7	SysAD7
6	D0:6	SysAD6
5	D0:5	SysAD5
4	D0:4	SysAD4
3	D0:3	SysAD3
2	D0:2	SysAD2
1	D0:1	SysAD1
0	D0:0	SysAD0

Table A.3 - Addr(Lo) Group Channel Assignments

A.5 CONTROL GROUP

The default radix of the group is **SYM** (symbolic); the associated symbol table is **R4000A_Ctrl**. The default radix for disassembly display is **OFF**.

The group and all channels as listed are required for use by the disassembler to produce a disassembly display.

The disassembler synthesizes the values displayed under the **R4000A Control** group column (independent of the channels' actual values) when subblock reordering is performed during display of assumed-instruction block read data cycles.

Refer to Table A.4.

Bit Position	Channel	Signal Name
11	C3:3	ResetB
10	C2:3*	ValidIn*
9	C2:2*	ValidOut*
8	C3:6	SysCmd8
7	C3:5	SysCmd7
6	C3:4	SysCmd6
5	C3:2	SysCmd5
4	C3:1	SysCmd4
3	C3:0	SysCmd3
2	C2:6	SysCmd2
1	C2:5	SysCmd1
0	C2:4	SysCmd0

Table A.4 - Control Group Channel Assignments

A.6 INTR GROUP

The default radix of the group is **SYM** (symbolic); the associated symbol table is **R4000A_Intr**. The default radix for disassembly display is **SYM**.

Neither the group itself nor the channels listed are required for use by the disassembler.

Refer to Table A.5.

Bit Position	Channel	Signal Name
1	C1:7	Int*_D
0	C1:6	NMI*

Table A.5 - Intr Group Channel Assignments

A.7 ACK GROUP

The default radix of the group is **SYM** (symbolic); the associated symbol table is **R4000A_Ack**. The default radix for disassembly display is **OFF**.

Neither the group itself nor the channels listed are required for use by the disassembler.

Refer to Table A.6.

Bit Position	Channel	Signal Name
1	C1:4	IvdErr*
0	C1:0	IvdAck*

Table A.6 - Ack Group Channel Assignments

A.8 MISC GROUP

The default radix of the group is **OFF**. The default radix for disassembly display is **OFF**.

Neither the group itself nor the channels listed are required for use by the disassembler.

Refer to Table A.7.

Bit Position	Channel	Signal Name
3	C1:3	ColdReset*
2	CK2*	Ivd*_D
1	CK1*	CmdRd*_D
0	CK0*	CmdWr*_D

Table A.7 - Misc Group Channel Assignments

A.9 CHK GROUP

The default radix of the group is **OFF**. The default radix for disassembly display is **OFF**.

Neither the group itself nor the channels listed are required for use by the disassembler.

Refer to Table A.8.

Bit Position	Channel	Signal Name
8	C1:2	SysCmdP
7	C0:7	SysADC7
6	C0:6	SysADC6
5	C0:5	SysADC5
4	C0:4	SysADC4
3	C0:3	SysADC3
2	C0:2	SysADC2
1	C0:1	SysADC1
0	C0:0	SysADC0

Table A.8 - Chk Group Channel Assignments

A.10 CLK GROUP

The default radix of the group is **OFF**. The default radix for disassembly display is **OFF**.

Neither the group itself nor the channel listed are required for use by the disassembler (except that the signal is used as the clocking source for the acquisition module).

Refer to Table A.9.

Bit Position	Channel	Signal Name
0	CK3	Clk

Table A.9 - Clk Group Channel Assignment

A.11 UNUSED GROUP

The default radix of the group is **OFF**. The default radix for disassembly display is **OFF**.

Neither the group itself nor the channels listed are required for use by the disassembler.

Refer to Table A.10.

Bit Position	Channel	Signal Name
3	Q1	Unused_Q1
2	Q0	Unused_Q0
1	C3:7	UnusedC3_7
0	C2:7	UnusedC2_7

Table A.10 - Unused Group Channel Assignments

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B. SOFTWARE WARRANTY AND SERVICE

This software product has a warranty against defects in the media for a period of one (1) year. During this warranty period, Crescent Heart Software will replace products that are defective. Please refer to the software licensing agreement printed on the envelop in which the floppy disk(s) were packaged for further information.

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For more information on probe adapters, SMT and BGA adapters, other disassemblers and other available items, please contact Crescent Heart Software or the distributor from whom this product was purchased.

Also contact Crescent Heart Software concerning any requirements you may have for custom modifications to this software product or for information concerning development of custom support software or hardware for probing other processors or related support devices.

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